NJICE –National Journal on Information and Communication Engineering
ISSN: 2231-2099Volume 11 Issue 1
Jan-March 2021 Pages 31-35

SBFET -Based Full Adder with Ultra-Low Leakage and High Speed

B.LAKSHMI[1]
Department of Electronics and Communication Engineering, A.R.Engineering College, Villupuram.
saranyameece@gmail.com
Number: +91-7708932286

N.MUTHU KUMARAN[2]
Department of Electronics and Communication Engineering, A.R.Engineering College, Villupuram.
n.muthukumaran.ece@gmail.com
Number: +91-7708363460

***Abstract*—The design of full adder has always been considered by designers over the years and the main efforts in this field have been on low operating voltage, low-power consumption, high speed, low chip area and high energy efficiency. For this purpose, in this paper, graphene nano-ribbon field effect transistors (SBFETs) that compete with conventional MOSFET technology due to their higher current drive capabilities, ballistic transport, lower power-delay product (PDP), and higher thermal stability, are used for designing a full adder. Based on the promising properties of SBFETs, an ultra-low-leakage and low-voltage full adder cell with 18 transistors is proposed. The proposed design utilizes the unique features of MOSFET-like SBFETs for high performance. The simulations were performed using Synopsys HSPICE with 16nm MOS-SBFET technology and the simulation results show the superiority of the SBFET-based design in terms of speed and PDP compared to conventional and modern structures even at 0.5V supply voltage.**

Keywords*—Ultra-low leakage, 1-bit full adder, Graphene nano-ribbon field effect transistor (SBFET), Power-delay product (PDP), Low-Voltage.

I. INTRODUCTION

Transistors are used as a major component in all electronic devices such as flash drives, laptop and desktop computers, radios, mobile phones and smartwatches. Due to the growing demand for electronic equipment, the production of high quality devices and various functions is important for electronic equipment manufacturers. As the scale of the MOSFET process in CMOS technology decreases, traditional silicon MOSFETs are no longer able to maintain Moore's law. Hence, engineers and scientists are trying to find a solution to overcome this challenge. One solution to this problem is to replace the conductor channels of MOSFETs with new materials such as silicon nanowires, carbon nanotubes, graphene, and graphene nano-ribbon [1]. According to reports published by International Technology Roadmap for Semiconductors ITRS, more research will be done on graphene and graphene nano-ribbon to replace silicon in the semiconductor industry, and it is predicted that traditional silicon will be replaced by graphene nano-ribbon in the coming years [2].

Since graphene was discovered by Novoselov et al. in 2004, many researchers have become interested in research in this field [3]. Graphene is an open form of carbon nanotube, and carbon-based families include fullerene, graphene, and graphene nano-ribbon. Due to the special structure and excellent properties of graphene, studies on its mechanical and electronic properties have been done in many articles and it is predicted that in the near future graphene will be used as one of the best candidates in nano-devices as a conductive channel. Due to the fact that graphene nano-ribbon and carbon nanotubes originate from the same source and the process of making graphene nano-ribbon is easier compared to carbon nanotubes, there is a lot of interest in studying the performance of graphene nano-ribbon.

The demand for a full adder design with low operating voltage, low power consumption, high speed, low chip area and high energy efficiency has always been of interest [1,4]. Due to the severe limitations of the nanometer-scale MOSFET, the use of MOSFET as a main unit in full adder has now reached its functional limitations such as average power dissipation and speed. Therefore, in this paper, a new one-bit full adder based on SBFET is presented, whose structure hasan extremely low leakage and has a very high performance.

The rest of this article is organized as follows. In the second part, the proposed full adder cell design based on SBFET is presented. In the third part, the simulation results are presented and in the fourth part, the article ends with a conclusion.

II. SBFET-BASED FULL ADDER DESIGN

Addition is the most important computational operation and is commonly used in any digital electronics and computational logic unit (ALU) to add any numeric value. Usually a one-bit adder cell is a full adder that has three inputs (A, B, and C_{in}), and when these three inputs are added together, the Sum and C_{OUT} outputs are generated. The

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relations for Sum and C_{OUT} outputs in a one-bit full adder are as follows:

$$Sum=A\oplus B\oplus C_{in} \quad (1)$$

$$C_{out}=A\cdot B+C_{in}\cdot(A\oplus B) \quad (2)$$

The above relations can be realized by using two XOR gates and a 2-to-1 multiplexer. For this purpose, the design of a full adder using two stages of XNOR gates or two stages of XOR gates to generate Sum logic and the use of a 2-to-1 multiplexer is presented in [5-7], which is a modular design. We will use this structure to simulate the proposed full adder. It is clear that the two XOR gates used in this structure play an important role in the speed and power consumption of the entire of full adder circuit. If the performance of these two XORs can be improved, it can improve the performance of the entire of full adder circuit. For this purpose, we will present a new and optimal XOR based on the SBFET and evaluate its performance inside the full adder. Fig. 1 shows a schematic of SBFET-based full adder. Here, the proposed XOR circuit implements the XOR function using six SBFETs and a capacitor. In Fig. 1, transistors M1 to M6 actas the first XOR circuit, and transistors M13 to M18 act as the second XOR circuit. This circuit implements the XOR function without the use of any complementary inputs. Also, this circuit has the shortest possible critical path. It should be noted that shortening the critical path of designs and implementing circuits without complementary inputs are the most efficient way to reduce delay and power consumption simultaneously. In the proposed XOR, transistors M5 and M6 (also, M17 and M18) are used to reduce the power consumption, which is based on the technique presented in [8]. It is worth noting that in the technique introduced in [8], in order to reduce the power, two transistors are used in series and in parallel with a capacitor in the downstream network to limit most of the leakage current of the full adder circuit.

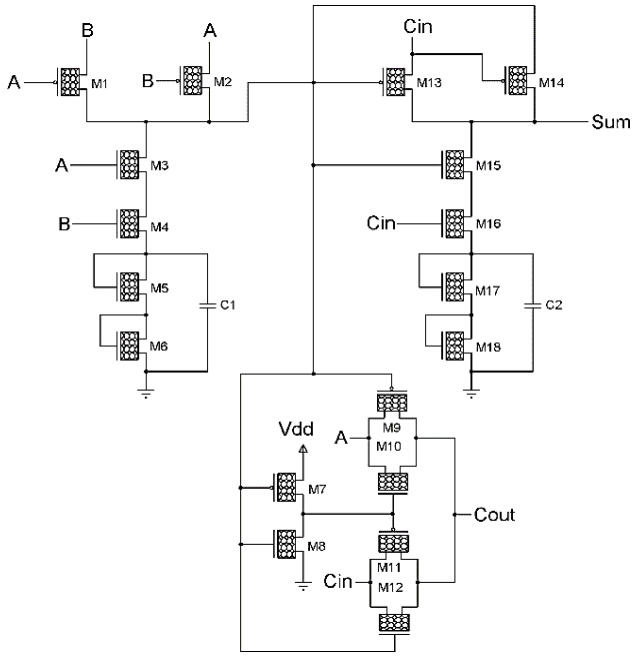

Fig. 1. Schematic of SBFET-based proposed full adder

III. Simulation Results

In this section, SBFET-based full adder was extensively evaluated in different situations. The proposed design was simulated by the University of Illinois with all non-idealities for a 16nm SBFET-based circuit using the Synopsys HSPICE simulation tool and the proposed model for the MOS-SBFET [9]. The model is designed for SBFET devices where each device may have one or more graphene nano-ribbon (GNR) (see Fig. 2). Since the various complex mechanisms that describe the region below 10 nm are not modeled here, the minimum channel length is approximately 10 nm. Also, this model is based on the assumption of ballistic transmission, which is only valid in a short channel SBFET. As a result, adjusting the channel length above 100 nm is not recommended. The channel width in the GNR network is determined by:

$$W_{ch} = \frac{(N+1)}{2}\sqrt{3}d_{cc} \quad (3)$$

where N is the number of dimer lines and d_{cc} = 0.142 nm refers to the carbon-carbon bond distance.

In practice, the channel width is unlimited. However, since the bandgaps of GNRs are inversely proportional to thewidth, a wide GNR has a small I_{on}/I_{off} ratio and will not be suitable for digital circuits. Therefore, widths up to about N = 50 are suggested. Gate width W_G in terms of W_{CH} is defined as:

$$W_G = (2W_{sp} + W_{CH}) \times n_{Rib} \quad (4)$$

where $2W_{sp}$ is the distance between the ribbons and n_{Rib} is the number of ribbons. Other parameters such as oxide thickness, line edge roughness and doping fraction (for MOS-SBFET) have been thoroughly tested within the limits specified in Table I.

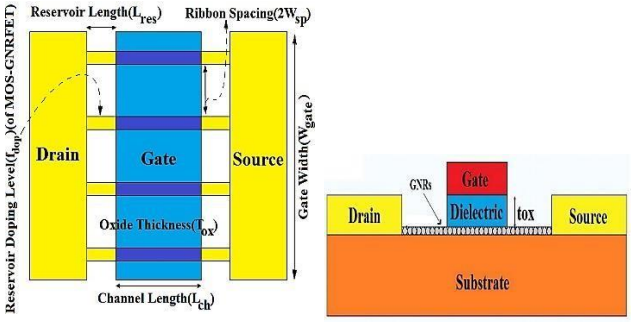

Fig. 2. Demonstration of MOS-SBFET

TABLE I. Summary of SBFET model parameters for P and N type SBFETs

Specification	Value
Maximum channel length (nm)	~ 100
Minimum channel length (nm)	~ 10

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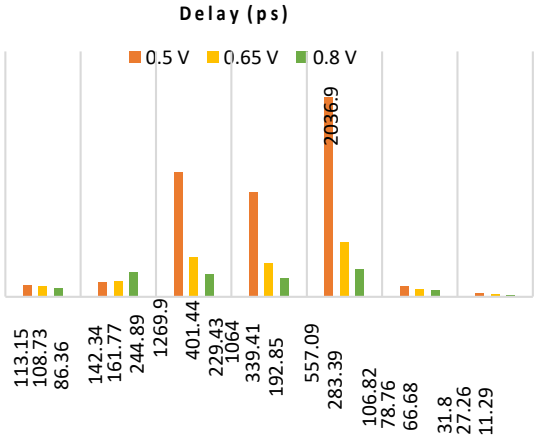
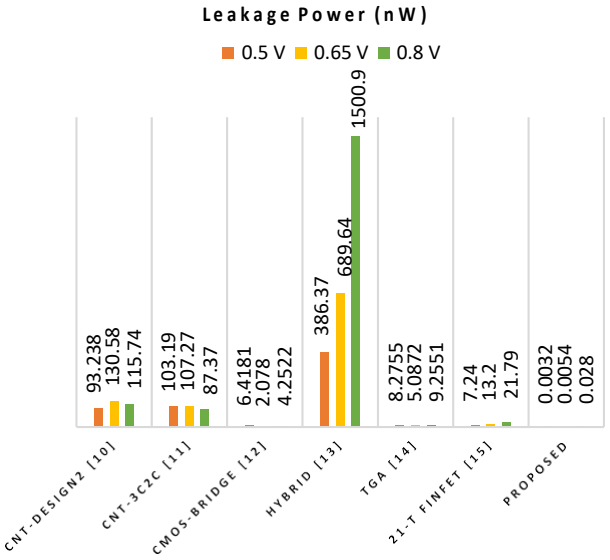
Maximum channel width (nm) per GNR	~ 6.36
Minimum channel width (nm) per GNR	~ 0.873
Maximum GNRs per device	unlimited
Minimum GNRs per device	1
Maximum oxide thickness (nm)	2.5
Minimum oxide thickness (nm)	0.5
Maximum line edge roughness (%)	20
Minimum line edge roughness (%)	0
Maximum doping fraction	0.015
Minimum doping fraction	0.001

Simulations of the proposed full adder were performed at 27°C with different supply voltages. In order to measure the propagation delay, a complete input pattern with all possible transitions from one input combination to another was applied to the full adder circuit. The delay was measured for

each transition and the maximum value of this measurement is reported as the propagation delay of full adder. Also, the average power consumption is measured in a periodic cycle and the product of this value with the maximum delay measured is considered as PDP. In this paper, we will consider the PDP value as an important criterion for evaluating and comparing the performance of proposed full adder with other structures.

SBFET-based proposed full adder were simulated at various supply voltages (0.8, 0.65 and 0.5 V) and at frequency of 100 MHz with capacitive loads of 2.2 fF in the outputs of full adder. The results of these simulations are shown graphically in Fig. 3 in terms of delay, average power consumption, leakage power and PDP and are compared with other traditional and modern works. According to the results shown in Fig. 3, the proposed full adder has the lowest delay, leakage power, average power consumption and extremely low PDP compared to previous designs at different supply voltages, which is unique in its kind.





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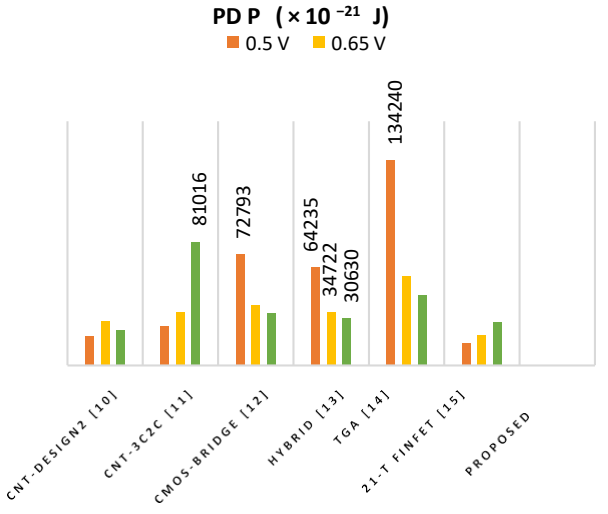

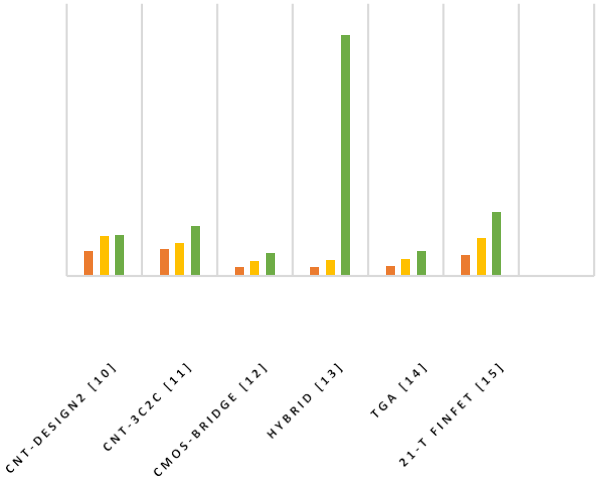

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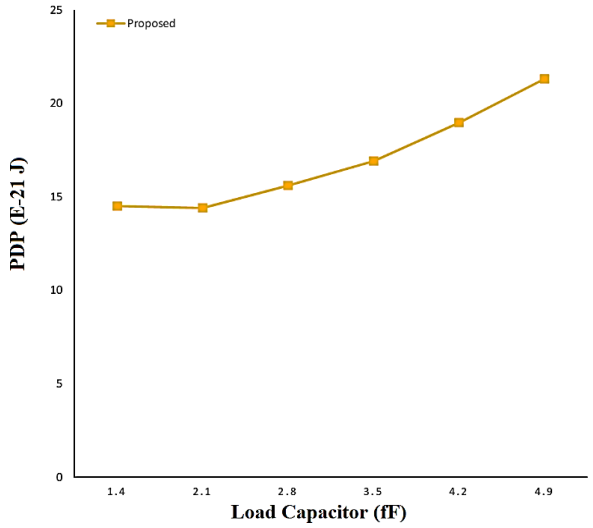
Fig. 3. Delay, average power consumption, leakage power and PDP of proposed full adder and comparison with other previous works (frequency of 100 MHz with capacitive loads of 2.2 fF)

In another experiment, we compared the performance of the proposed full adder with other designs in the same conditions at three different supply voltages (0.8, 0.65 and 0.5V) with a frequency of 375 MHz and a capacitive load of 3.5 fF. The results of this test are listed in Table II. Experimental results show that our proposed design has the lowest delay, and average power consumption and ultra-low PDP compared to other designs at all voltages. Other designs cannot work well at 0.5V supply voltage, while the proposed design can maintain its performance well.

TABLE II. DELAY, AVERAGE POWER CONSUMPTION AND PDP OF PROPOSED FULL ADDER AND COMPARISON WITH OTHER PREVIOUS WORKS (FREQUENCY OF 375 MHZ WITH CAPACITIVE LOADS OF 3.5 FF)

V_{dd} (v)	0.5	0.65	0.8
Delay (ps)			
CNT-Design2 [10]	241.96	568.93	160.92
CNT-3c2c [11]	344.93	547.27	Failed
CMOS-Bridge [12]	Failed	526.37	308.92
Hybrid [13]	Failed	484.81	292.86
TGA [14]	Failed	815.32	415.14
21-T FinFET [15]	160.92	126.16	101.84
Proposed	**71.41**	**35.69**	**19.79**
Average power (nW)			
CNT-Design2 [10]	484.16	863.37	1087.12
CNT-3c2c [11]	522.81	919.63	Failed
CMOS-Bridge [12]	Failed	569.13	906.83
Hybrid [13]	Failed	612.51	986.17
TGA [14]	Failed	577.17	964.17
21-T FinFET [15]	628.38	1184.59	1965.28
Proposed	**1.477**	**3.404**	**5.087**
PDP (aJ)			
CNT-Design2 [10]	117.147	491.197	174.939
CNT-3c2c [11]	180.3328	503.2859	Failed
CMOS-Bridge [12]	Failed	299.572	280.137
Hybrid [13]	Failed	296.950	288.809
TGA [14]	Failed	470.578	400.265
21-T FinFET [15]	101.118	149.447	200.144
Proposed	**0.001055**	**0.001215**	**0.001006**

In the other test, drivability of the proposed full adder and other previous designs with different capacitive loads at frequency of 100 MHz and supply voltage of 0.65 V was evaluated. PDP of full adder circuits are plotted in Fig. 4 in terms of capacitive load changes from 2.1 fF to 4.7 fF. Based on the results shown in Fig. 5, PDP of the proposed full adder is lower than the PDP of other circuits for all capacitive loads. To evaluate the proposed design's immunity to ambient temperature changes and to compare it with other previous designs, these circuits were simulated from 0 °C to 100 °C. The results of the immunity test against changes in ambient temperature are shown in Fig. 5. It can be inferred that the SBFET-based design has acceptable performance and its PDP is extremely low compared to other designs at all temperatures.



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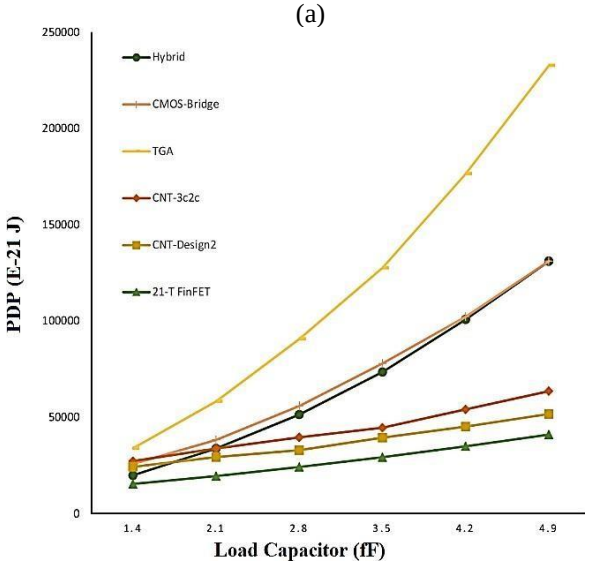
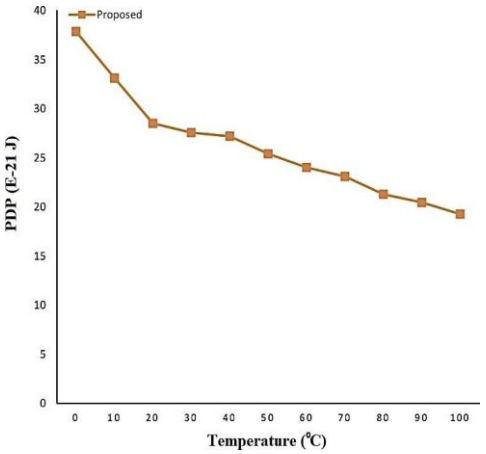


(b)

Fig. 4. PDP of different full adder circuits in terms of output load change



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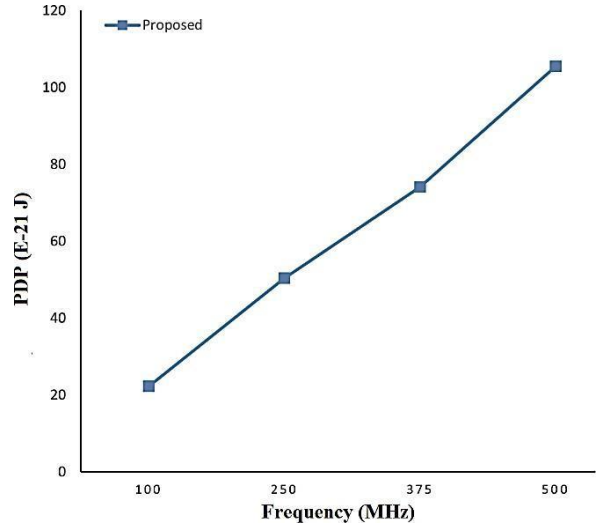
In final test, we evaluate the effect of frequency change on the proposed design and compare it with other previous designs, different full adder circuits were simulated at different frequencies from 100 MHz to 500 MHz and supply voltage of 0.65 V. The results of the frequency change and its effect on the various designs are shown in Fig. 6. It shows that the proposed SBFET-based full adder operate normally at different frequencies and it can operate reliably and with low power consumption at various frequencies. Also, it can be inferred from the results that the SBFET- based design has the lowest average power consumption at various frequencies and its power consumption is less compared to other circuits with increasing frequency.



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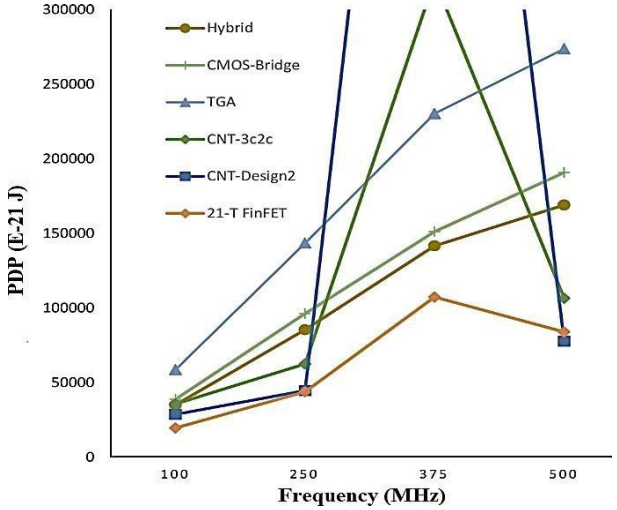

(b)

Fig. 6. PDP of various full adder circuits in terms of operating frequency

IV. Conclusion

In this paper for low-voltage applications, an ultra-low leakage full adder cell with high speed and efficiency using SBFETs is proposed. The simulation results show a significant improvement in terms of delay and PDP in different situations. According to the performed simulations in supply voltage of 0.8 V, frequency of 100 MHz and capacitive load of 2.1 fF, propagation delay of 11.29 ps, average power of 0.84 nW, leakage power of 0.028 nW and PDP of 9.49 $\times 10^{-21}$ J were obtained for proposed full adder with 16 nm MOS-SBFET technology. The proposed full adder can be reliably used in supply voltage of 0.5 V. Based on the obtained results in supply voltage of 0.5 V, frequency of 100 MHz and capacitive load of 2.1 fF, propagation delay of 31.80 ps, average power of 0.318 nW, leakage power of 0.0032 nW and PDP of 23.656×10^{-21} J. It should be noted that the scope of this paper is to introduce SBFET technology and its significant advantages over MOSFET technology to encourage electronics designers to do research in this field.

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